WE CLAIM:

1. A method of depositing a non-epitaxial silicon layer on a substrate within a reaction chamber at a pressure of a greater than about 500 Torr, comprising flowing process gases through the reaction chamber and over the substrate at a desired reaction temperature, with a process gas residence time in the reaction chamber of less than about 100 seconds.

2. The method of Claim 1, wherein the residence time is less than about 60 seconds.

3. The method of Claim 2, wherein the residence time is less than about 20 seconds.

4. The method of Claim 1, wherein the pressure is greater than about 700 Torr.

5. The method of Claim 1, wherein the reaction chamber comprises a single-wafer horizontal reaction chamber having a constant height above the wafer in a cross-section taken along a gas flow axis.

6. The method of Claim 5, wherein the reaction chamber is vertically divided by a horizontal divider plate upstream and downstream of the substrate, the divider plate approximately in the plane of the substrate.

7. The method of Claim 1, wherein the process gases comprise silane and hydrogen.

8. A process for depositing a non-epitaxial silicon layer by chemical vapor deposition, comprising:

placing a substrate into a single-wafer processing reaction chamber;

raising the temperature of the substrate to a reaction temperature between about 625°C and 850°C;

introducing process gases including a silicon source gas and a hydrogen carrier gas to the reaction chamber; and

flowing the process gases over the substrate while maintaining the reaction chamber at a pressure of greater than about 700 Torr.

9. The process of Claim 8, wherein polysilicon is deposited at a rate of at least about 50 nm/min.

10. A method of depositing silicon by chemical vapor deposition, comprising:

loading a semiconductor substrate into a reaction chamber, the substrate including a plurality of holes therein, the holes having openings of no more than about 0.5 μm and aspect ratios of greater than about 2:1;

ramping the substrate temperature to a desired reaction temperature;

maintaining a pressure of greater than about 700 Torr in the reaction chamber; and

flowing a silane-based silicon source gas, a hydrogen carrier gas, and a dopant source gas simultaneously over the substrate within the reaction chamber at the desired reaction temperature, thereby depositing an *in situ* conductively doped silicon layer over the substrate and into the holes, wherein the silicon layer exhibits greater than about 70% step coverage of the holes.

11. The method of Claim 10, wherein the silicon layer exhibits greater about 80% step coverage of the holes.

12. The method of Claim 10, wherein the silicon layer exhibits greater about 85% step coverage of the holes.

13. The method of Claim 12, wherein the silicon layer exhibits greater about 90% step coverage of the holes.

14. The method of Claim 10, wherein the desired reaction temperature is greater than about 650°C.

15. The method of Claim 14, wherein the desired reaction temperature is less than about 700°C.

16. The method of Claim 10, wherein the silicon source gas comprises monosilane.

17. The method of Claim 10, wherein the holes have an aspect ratio of greater than about 5:1.

18. The method of Claim 10, wherein the holes have an aspect ratio of greater than about 10:1.

19. The method of Claim 10, wherein the holes have an aspect ratio of greater than about 20:1

20. The method of Claim 10, wherein the holes have an aspect ratio of greater than about 40:1.

21. The method of Claim 10, wherein the deposited silicon layer incorporates arsenic.

22. The method of Claim 10, wherein depositing the silicon layer comprises growing the layer at greater than about 50 nm/min.

23. The method of Claim 10, wherein depositing the silicon layer comprises growing the layer at greater than about 100 nm/min.

24. A method of forming an integrated circuit, comprising:

providing a substrate with a hole having greater than a 2:1 aspect ratio;

loading the substrate into a single-wafer processing chamber;

depositing silicon into the hole at a rate of at least about 50 nm/min with greater than about 80% step coverage.

25. The method of Claim 24, wherein depositing silicon comprises flowing silane in a hydrogen carrier gas.

26. The method of Claim 24, wherein the aspect ratio of the hole is greater than about 5:1.

27. The method of Claim 26, wherein the aspect ratio of the hole is greater than about 10:1.

28. The method of Claim 27, wherein depositing silicon includes *in situ* doping.

29. The method of Claim 28, wherein *in situ* doping comprises flowing arsine.

30. The method of Claim 29, wherein depositing silicon comprises maintaining the chamber at a pressure greater than about 500 Torr.

31. The method of Claim 30, wherein depositing silicon comprises maintaining the chamber at about atmospheric pressure.

32. The method of Claim 31, wherein flowing said hydrogen carrier gas and silane comprises maintaining a reactant residence time in the reaction chamber of less than about 100 seconds.

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33. An integrated capacitor formed in trench having a width of no more than about 0.25 μm and an aspect ratio greater than about 20:1, comprising:

a dielectric layer lining the trench; and

a conductively doped polysilicon layer filling the trench.

34. The integrated capacitor of Claim 33, wherein the conductively doped polysilicon layer comprises arsenic.

35. The integrated capacitor of Claim 33, wherein the trench has a depth of greater than about 5 μm.

36. The integrated capacitor of Claim 35, wherein the trench has a depth of greater than about 7 μm.

37. The integrated capacitor of Claim 36, wherein the trench is formed in a semiconductor substrate.